

CMPU-224 Lab9 Quiz

Spring 2026

Name: _____

This is a closed book, closed notes quiz. No electronic devices are allowed. You have until 3:30pm to complete the quiz. There are a total of 9 questions and 10 points.

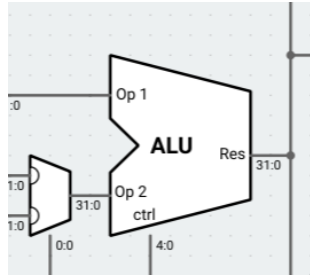
There should be enough space on the quiz for your answers. If you need more space to work out a problem, blank paper will be available, just ask.

If you finish with time remaining, raise your hand and I will come and collect your quiz. You may then work on the lab assignment.

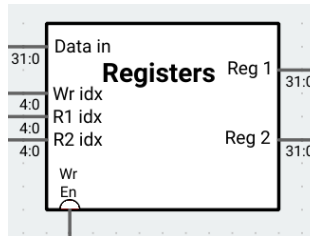
Good Luck!

1. (1 point) The RV32I single-cycle datapath is conceptually divided into five stages. Which of the following lists them in the correct order from first to last?
 - A. Decode, Fetch, Execute, Write-Back, Memory
 - B. Fetch, Decode, Execute, Memory, Write-Back
 - C. Fetch, Execute, Decode, Write-Back, Memory
 - D. Fetch, Decode, Memory, Execute, Write-Back
2. (1 point) Which RISC-V instruction determines the minimum clock period (i.e., defines the critical path) of the single-cycle processor because it is the only instruction that meaningfully exercises all five stages?
 - A. `add`
 - B. `addi`
 - C. `lw`
 - D. `beq`

3. (1 point) When executing `addi t1, t0, -25`, the MUX in front of the ALU's second operand input must select which value?



- A. The value read from register `rs2`
 B. The sign-extended 12-bit immediate
 C. The current value of the PC
 D. The value read from register `rd`
4. (2 points) Consider the instruction `add x5, x6, x7`. During its execution, what signals are driven into the Register File's two read-port address inputs (R1 idx and R2 idx)? Give your answer as an unsigned decimal number.



R1 idx = _____

R2 idx = _____

5. (1 point) For a `lw` instruction, what does the Write-Back MUX (the MUX immediately before the register file's *Data in* write port) select?
- A. The ALU result
 B. The data read from Data Memory
 C. The value `PC + 4`
 D. The sign-extended immediate

6. (1 point) The MUX in front of the PC register selects the next value of the PC each cycle. Which of the following correctly lists *all* the inputs to that MUX in the RV32I single-cycle datapath?
- A. PC + 4 only
 - B. PC + 4 and the output from the immediate generator
 - C. PC + 4 and the value read from Data Memory
 - D. PC + 4 and the ALU result
7. (1 point) During the execution of `beq t0, t1, equal`, the values of `t0` and `t1` are both 5. What value does the PC-select MUX pass to the PC register on the next rising clock edge?
- A. PC + 4
 - B. PC + `offset`
 - C. `rs1 + immediate`
 - D. `rs2 + immediate`
8. (1 point) A **transparent** (level-sensitive) latch and an **edge-triggered** latch differ in *when* they capture the value on their data input D. Which statement correctly describes the difference?
- A. Both types capture D continuously while the clock is high.
 - B. A transparent latch captures D while the clock is high and latches the value as the clock falls; an edge-triggered latch captures D only at the instant of the rising clock edge.
 - C. An edge-triggered latch captures D while the clock is high; a transparent latch captures D only on the rising edge.
 - D. Both types capture D only on the rising clock edge.
9. (1 point) In a register file, reading and writing behave differently with respect to the clock. Which of the following correctly describes this difference?
- A. Both reads and writes are clocked: output data appears only on the rising clock edge.
 - B. Both reads and writes are combinational: output data changes continuously as the address input changes.
 - C. Reads are combinational (output data appears after a propagation delay whenever the address changes); writes are clocked (the selected word is updated only on the rising clock edge).
 - D. Reads are clocked; writes are combinational.